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REMARKS

After entry of this amendment, claims 1-49 are pending. In the present Office Action, claims 2-5, 9-12, 16-19, and 22-25 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3, 5-10, 12-17, 19-23, and 25-26 were rejected under 35 U.S.C. § 102(b) as being anticipated by Turley (Advanced 80386 Programming Techniques) ("Turley"). Claims 4, 11, 18, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Blomgren, U.S. Patent No. 5,826,074 ("Blomgren"). Applicant respectfully traverses these rejections and requests reconsideration.

Claims 1-38

Applicant respectfully submits that each of claims 1-38 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "a plurality of segment registers including a code segment register and a stack segment register; a circuit configured to generate an indication of a default operand size …wherein, in a first operating mode … , each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and an execution core … configured, in the first operating mode, to override the default operand size with a second operand size responsive to the first instruction having an implicit stack pointer reference".

The present Office Action asserts that Turley teaches an execution core configured to "override the default operand size with a second operand size responsive to the first instruction have an implicit stack pointer reference", referring to the use of the D bit from the segment descriptor indicated by the stack segment register (SS) for instructions that have implicit stack pointer references. Specifically, the Office Action states that the D bit of the stack segment descriptor overrides the D bit of the code segment descriptor for such instructions. See Office Action, page 4, lines 7-15.

Applicant respectfully submits that Turley's teachings regarding using the stack segment register/descriptor to determine the address size for implicit stack references do not teach or suggest "a plurality of segment registers including a code segment register

and a stack segment register; a circuit configured to generate an indication of a default operand size ...wherein, in a first operating mode ... , each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and an execution core ... configured, in the first operating mode, to override the default operand size with a second operand size responsive to the first instruction having an implicit stack pointer reference".

For at least the above stated reasons, Applicant respectfully submits that claim 1 is patentable over the cited art. Claims 2-7 and 27-29 depend from claim 1, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 2-7 and 27-29 recite additional combinations of features which are not taught or suggested in the cited art.

Claim 8 recites a combination of features including: "the code segment register is one of a plurality of segment registers that also includes a stack segment register, and wherein the segment descriptor further indicates an operating mode, and wherein each other one of the plurality of segment registers except for the code segment register is ignored in the operating mode for providing segment data; and overriding the default operand size with a second operand size for a first instruction, in the operating mode, responsive to the first instruction having an implicit stack pointer reference". The teachings of Turley, highlighted above with regard to claim 1, also do not teach or suggest the above highlighted features of claim 8.

For at least the above stated reasons, Applicant respectfully submits that claim 8 is patentable over the cited art. Claims 9-14 and 30-32 depend from claim 8, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 9-14 and 30-32 recite additional combinations of features which are not taught or suggested in the cited art.

Claim 15 recites a combination of features including: "a plurality of segment registers including a code segment register and a stack segment register; a circuit

configured to generate an indication of a default operand size... and wherein, in a first operating mode ..., each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and an execution core coupled to receive a near branch instruction, wherein the execution core is configured to override the default operand size with a second operand size responsive to the near branch instruction in the first operating mode".

With regard to claim 15, the Office Action again relies on Turley's teachings referring to the use of the D bit from the segment descriptor indicated by the stack segment register (SS) for instructions that have implicit stack pointer references. Specifically, the Office Action states that the D bit of the stack segment descriptor overrides the D bit of the code segment descriptor for such instructions. Furthermore, the Office action asserts that the CALL instruction has an implicit stack reference and also may be a near branch instruction. See Office Action, page 11, lines 1-15.

Applicant respectfully submits that Turley's teachings regarding using the stack segment register/descriptor to determine the address size for CALL instructions does not teach or suggest "a plurality of segment registers including a code segment register and a stack segment register; a circuit configured to generate an indication of a default operand size... and wherein, in a first operating mode ..., each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data; and an execution core coupled to receive a near branch instruction, wherein the execution core is configured to override the default operand size with a second operand size responsive to the near branch instruction in the first operating mode".

For at least the above stated reasons, Applicant respectfully submits that claim 15 is patentable over the cited art. Claims 16-20 and 33-35 depend from claim 15, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 16-20 and 33-35 recite additional combinations of features which are not taught or suggested in the cited art.

Claim 21 recites a combination of features including: "the code segment register is one of a plurality of segment registers that also includes a stack segment register, and wherein the segment descriptor further indicates an operating mode, and wherein each other one of the plurality of segment registers except for the code segment register is ignored in the operating mode for providing segment data; and overriding the default operand size, in the operating mode, with a second operand size for a near branch instruction". The teachings of Turley, highlighted above with regard to claim 15, also do not teach or suggest the above highlighted features of claim 21.

For at least the above stated reasons, Applicant respectfully submits that claim 21 is patentable over the cited art. Claims 22-26 and 36-38 depend from claim 21, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 22-26 and 36-38 recite additional combinations of features which are not taught or suggested in the cited art.

New Claims 39-49

New claims 39-49 each recite a combination of features not taught or suggested in the cited art. For example, claim 39 recites a combination of features including: "the plurality of segment registers include a code segment register and a stack segment register; and a processor configured to generate an indication of a default operand size, ... wherein, in a first operating mode ..., each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data, and wherein, in response to a first instruction having an implicit stack reference and the first operating mode, the processor is configured to override the default operand size with a second operand size". Claims 40-44 depend from claim 39. Claim 45 recites a combination of features including: "the plurality of segment registers include a code segment register and a stack segment register; and a processor configured to generate an indication of a default operand size, wherein the processor is configured to generate the default operand size ... wherein, in a first operating mode ..., each other one of the plurality of segment registers except for the code segment register is ignored for providing segment data, and wherein the processor is configured to override the default

operand size with a second operand size responsive to a near branch instruction in the first operating mode". Claims 46-49 depend from claim 45.

Section 112 Rejection/Drawing Objection

The section 112 rejection is based on the use of the term "configuration register" in claims 2, 4, 9, 16, 18, and 22. Applicant respectfully submits that this term is clear to one of skill in the art, and respectfully traverse the rejection. Nevertheless, Applicant has amended the above claims to recite a "control register" rather than a "configuration register". Applicant submits that the term "control register" is clear, and further that the term "control register" may be found throughout the present specification. For example, see page 5, line 24.

The drawings were objected for not showing a configuration register. As mentioned above, the term "configuration register" has been changed to "control register". Fig. 1, for example, shows a number of control registers (e.g. reference numerals 26 and 28). Accordingly, Applicant submits that the drawing objection should be removed.

Declaration Objection

The Office Action objected to the declaration as defective for stating that a provisional priority claim was not applicable when there is a priority claim to provisional application serial no. 60/224,368. The Office Action referred to MPEP 602.01 and 602.02 in the objection. Applicant submits that nothing in MPEP 602.01 and 602.02 requires that the declaration identify a priority claim to a provisional application. Rather, MPEP 602 requires that FOREIGN priority claims be included in the declaration (or in an application data sheet), but is silent on the issue of priority claims to provisional patent applications. Applicant is aware of no requirement to include the priority claim to a provisional application in the declaration, even if the declaration includes a space to insert such a claim. Applicant also notes that the current declaration form provided by the Office (PTO/SB/01) includes a section for foreign priority claims, but no section for provisional application priority.

Accordingly, Applicant submits that the declaration is not defective and furthermore that priority to the provisional application is properly claimed in the present application. Nevertheless, Applicant includes herewith a Supplemental Declaration including the priority claim.

Previously Submitted Request to Rescind

The Office Action acknowledged the preliminary amendment, request for corrected filing receipt, and information disclosure statement filed in the above-captioned application. However, no mention is made of the Request to Rescind Previous Non-Publication Request. Applicant filed the Request to Rescind on September 21, 2001. Attached hereto as Exhibit A is a copy of the previously-filed Request to Rescind, along with a copy of the date-stamped postcard evidencing receipt of the Request to Rescind in the United States Patent and Trademark Office on September 25, 2001. Applicant respectfully requests acknowledgement of the Request to Rescind in the next action.

CONCLUSION

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66300/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

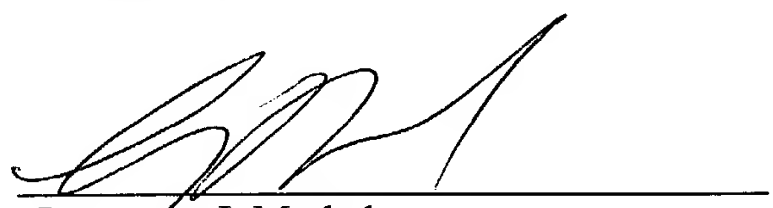
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☒ Please debit the deposit account identified above in the amount of $604 for fees ($172 for 2 excess independent claims and $432 for 24 excess claims over 20).

☒ Other: Supplemental Declaration; IDS and references; and Exhibit A: Previously submitted Request to Rescind and copy of date-stamped post card.

Respectfully submitted,



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